DIPANJAN SENGUPTA

Apt #2318, 116 Ponce De Leon NE
Altanta, GA 30308

Phone: **313-460-4592**
Email: *dsengupta6@gatech.edu*

RESEARCH INTERESTS:

Big Data, Graph Analytics, Machine Learning, Operating Systems, Computer Architecture, Virtualization, High-Performance Computing.

EDUCATION:

Georgia Institute of Technology, Atlanta, GA Aug 2011 - Present
Ph.D. candidate, Computer Science
Advisor: Prof. Karsten Schwan

Indian Institute of Technology (IIT) Kharagpur, India May 2004 - June 2008
B.Tech in Computer Science and Engineering

RESEARCH EXPERIENCE:

Georgia Institute of Technology, Atlanta Aug 2011 - Present
Graduate Research Assistant, CERCS
System Design Principles for Memory Management and Scheduling in Accelerator-based Systems

Indian Institute of Technology (IIT) Kharagpur Jan 2007 - May 2008
B.Tech Thesis
Design and implementation of a Secure File System (SFS) that pushes encryption services inside the Linux kernel, mounting it between the Virtual File System (VFS) layer and underlying filesystem.

PUBLICATION/PATENTS

- "GraphReduce: Processing Large-Scale Graphs on Accelerator-Based Systems"; **Dipanjan Sengupta**, Shuaiwen Leon Song, Kapil Agarwal, Karsten Schwan. [To appear in SC 2015].
- "GraphReduce: Large-Scale Graph Analytics on Accelerator-Based HPC Systems"; **Dipanjan Sengupta**, Kapil Agarwal, Shuaiwen Leon Song, Karsten Schwan. In Parallel and Distributed Processing Symposium Workshop (IPDPSW), 2015, Hyderabad, India May 2015.
- "A Framework for Emulating Non-Volatile Memory Systems with Different Performance Characteristics"; **Dipanjan Sengupta**, Qi Wang, Haris Volos, Ludmila Cherkasova, Jun Li, Guilherme Magalhaes and Karsten Schwan; ICPE 2015, Austin, TX, Jan 2015.
- "Scheduling Multi-tenant Cloud Workloads on Accelerator-based Systems"; **Dipanjan Sengupta**, Anshuman Goswami, Karsten Schwan, Krishna Pallavi; SC '14 New Orleans, LA, Nov 2014.
- "Multi-tenancy on GPGPU-based Servers"; **Dipanjan Sengupta**, Raghavendra Belapure, Karsten Schwan; VTDC '13, New York , NY, June 2013.
- "Method and Apparatus for an Improved Workflow for Digital Image Editing"; Swarnima Bansal, **Dipanjan Sengupta**. Patent issued US8655112 B2, Feb 2014.

WORK EXPERIENCE:

Intel Labs, Hillsboro, OR May 2015 - Aug 2015
Research Intern
Designed and implemented GraphIn, a high-performance graph analytics framework for evolving graphs.

HP Labs, Palo Alto, CA May 2014 – Dec 2014
Research Intern
Designed and developed a performance emulation platform for next-generation non-volatile memory (NVM) using commodity hardware.

Intel Corporation, Hillsboro, OR May 2013 - Aug 2013

Research Intern
As a part of Intel's X-Stack project team, designed and developed abstractions for open source Open Community Runtime (OCR) on Intel's Traleika Glacier architecture.

NEC Laboratories America, Princeton, NJ May 2012 - Aug 2012
Research Intern
Designed and implemented an efficient data transfer library, using Intel's Co-processor Offload Infrastructure (COI), to transfer data, over PCI Express, between host machine and Intel's Many Integrated Core (MIC).

Adobe Systems, India Dec 2008 - June 2011
Senior Software Developer in Adobe Photoshop® Elements team

- Designed and implemented *Photomerge Style transfer* and *Smart brsuh with effects* features in Adobe Photoshop® Element(PSE).
- Designed and implemented a resolution based **automatic application scaling algorithm** with lower bound of scaling factor proportional to the minimum application font size, in PSE 8.

NucleoDyne Systems Inc. Cupertino May 2007 – July 2007
Summer Intern
Development of embedded Linux kernel and configuring JFFS2 filesystem on top of custom designed Biophysical Oceanographic Sensor Array (BIOSA) embedded Board, Monterey Bay Aquarium Research Institute (MBARI).

SEMESTER PROJECTS:

- Implemented **Adaptive per-Thread Least-Attained-Service (ATLAS) and Thread Cluster (TCM)** memory scheduling algorithms in macsim simulator.
- Designed and implemented a trace driven superscalar, pipelined, speculative, hyper-threaded processor and memory system simulator.
- Designed a **4-bit microprogram controlled CPU** using IC chips, capable of performing elementary arithmetic/logic operations.

ACADEMIC HONORS:

- **Best student paper** finalist for SC '15.
- **All-India Rank (AIR) of 45** in the prestigious **IIT JEE examination 2004** among over 170,000 students all over India in 2004.
- **Goralal Syngal Memorial Scholarship** for securing **1st** position in the department of Computer Science and Engineering, in terms of AIR.
- **Adobe Spot Bravo Award** for the design and implementation of an **algorithm to automatically scale various UI elements based on system resolution** in Photoshop Elements 8.

SOFTWARE/PROGRAMMING SKILLS:

- Software Platforms: Linux, Solaris, Windows, Symbian
- Hardware Platforms: 8085, 80x86/x86 64, NVIDIA GPGPU, Intel MIC, JTAG debugger.
- Languages: C, C++, Intel x86 Assembly, Shell scripting, Python.
- Libraries: POSIX IPC, NVIDIA CUDA, Intel COI, Intel SCIF, Intel Cilk, OpenMP, MPI, BSD Sockets, OCR.

RELEVANT COURSES:

- **Graduate:** High-Performance Computer Architectures, Advanced Operating Systems, High Performance-Parallel Computing, Distributed Computing, Computer Networks, Computational Complexity Theory, Statistical methods.
- **Undergraduate:** Operating System, Computer Architecture, Computer Networks, Algorithms, Principles of Microprocessors, Compiler Design, Parallel Algorithms, Database Management Systems, Cryptography and Network Security, Applied Graph Theory, Testing and Verification of Circuits, Formal Languages and Automata Theory.